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Search Results -

Terms	Documents
L5 and (HIGH or LOW) with logic	11

09/747,734

Examiner: T. R. Sindram

Database:
- US Patents Full Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L6 and user with defin$4

Refine Search | Recall Text | Clear

Search History

DATE: Monday, May 06, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L6	L5 and (HIGH or LOW) with logic	11	L6
L5	L4 and write with enable	12	L5
L4	L3 and fail$3	13	L4
L3	L1 and control$5 with input and process with corner	19	L3
L2	L1 and control$5 with input and track$3 with process with corners	0	L2
L1	integrated near circuit and test$3 with (circuit or signal) and pulse with width	2873	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
test$3 near SRAM and self with tim$3 and write with stress	0

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L32

Refine Search

Recall Text | Clear

Search History

DATE: Sunday, May 19, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L32	test$3 near SRAM and self with tim$3 and write with stress	0	L32
L31	test$3 near memory and self with tim$3 and write with stress with mode	0	L31
L30	test$3 with memory near device and self with tim$3 with write with stress with mode	0	L30
L29	test$3	719782	L29
L28	L26 and ((324/$)!.CCLS.)	3	L28
L27	L26 and (built with in with test with circuit or BIST)	0	L27
L26	SRAM and test ADJ signal with pulse ADJ width	9	L26
L25	L23 and test ADJ signal with pulse ADJ width	0	L25

L24	L23 and ((324/$)!.CCLS.)	0	L24
L23	L22 and HIGH near logic and LOW near logic	26	L23
L22	L21 and (SRAM or static with random with access with memory)	26	L22
L21	L15 and configuration with input	26	L21
L20	L15 and predict$4 same fail$4	0	L20
L19	L15 and predict$4 with fail$4	0	L19
L18	L15 and fuse	0	L18
L17	L15 and fuse same program$5	0	L17
L16	L15 and fuse with program$5	0	L16
L15	L14 and transition	26	L15
L14	L13 and user with program$5	26	L14
L13	L12 and user with defin$5	27	L13
L12	L11 and fail$3	38	L12
L11	L10 and (HIGH or LOW) with logic	50	L11
L10	L8 and write with enable	55	L10
L9	L8 and process with corner$4	0	L9
L8	L7 and control$4 with input	88	L8
L7	L6 and pulse with width	102	L7
L6	BIST or (Built-in near test near circuit or built near in near test near circuit)	977	L6
L5	L4 and (HIGH or LOW) with logic	11	L5
L4	L3 and write with enable	12	L4
L3	L2 and fail$3	13	L3
L2	L1 and control$5 with input and process with corner	19	L2
L1	integrated near circuit and test$3 with (circuit or signal) and pulse with width	2878	L1

END OF SEARCH HISTORY

WEST

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Search Results -

Terms	Documents
SRAM and test ADJ signal with pulse ADJ width	9

Database: US Patents Full-Text Database
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Search: L26 and (324/$)!.CCLS.

Refine Search

Recall Text | Clear

Search History

DATE: Sunday, May 19, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L26	SRAM and test ADJ signal with pulse ADJ width	9	L26
L25	L23 and test ADJ signal with pulse ADJ width	0	L25
L24	L23 and ((324/$)!.CCLS.)	0	L24
L23	L22 and HIGH near logic and LOW near logic	26	L23
L22	L21 and (SRAM or static with random with access with memory)	26	L22
L21	L15 and configuration with input	26	L21
L20	L15 and predict$4 same fail$4	0	L20
L19	L15 and predict$4 with fail$4	0	L19
L18	L15 and fuse	0	L18
L17	L15 and fuse same program$5	0	L17
L16	L15 and fuse with program$5	0	L16
L15	L14 and transition	26	L15
L14	L13 and user with program$5	26	L14
L13	L12 and user with defin$5	27	L13
L12	L11 and fail$3	38	L12
L11	L10 and (HIGH or LOW) with logic	50	L11
L10	L8 and write with enable	55	L10
L9	L8 and process with corner$4	0	L9
L8	L7 and control$4 with input	88	L8
L7	L6 and pulse with width	102	L7
L6	BIST or (Built-in near test near circuit or built near in near test near circuit)	977	L6
L5	L4 and (HIGH or LOW) with logic	11	L5
L4	L3 and write with enable	12	L4
L3	L2 and fail$3	13	L3
L2	L1 and control$5 with input and process with corner	19	L2
L1	integrated near circuit and test$3 with (circuit or signal) and pulse with width	2878	L1

END OF SEARCH HISTORY